CLAIMS

WHAT IS CLAIMED:

1. A method of forming an SRAM memory cell, comprising:

forming a plurality of transistors above a semiconducting substrate;

forming a layer comprised of boron phosphosilicate glass (BPSG) above said substrate and said transistors;

forming a dielectric layer above said BPSG layer, said dielectric layer comprised of a material having a dielectric constant greater than approximately 6.0;

forming a plurality of openings in said dielectric layer and said BPSG layer, each of said openings allowing contact to a doped region of one of said transistors; and

forming a conductive local interconnect in each of said openings.

2. The method of claim 1, wherein forming said BPSG layer comprises performing at least one of a chemical vapor deposition process, a plasma enhanced chemical vapor deposition process and an atomic layer deposition process.

3. The method of claim 1, wherein forming said BPSG layer comprises depositing said BPSG layer to a thickness that ranges from approximately 150-200 nm.

4. The method of claim 1, wherein forming said BPSG layer comprises depositing said BPSG layer to a thickness such that an upper surface of said BPSG layer extends above an upper surface of one of said transistors by approximately 50-100 nm.

5. The method of claim 1, wherein forming a dielectric layer comprises performing at least one of a chemical vapor deposition process, a plasma enhanced chemical vapor deposition process, an atomic layer deposition process and a spin-coating process.

6. The method of claim 1, wherein said dielectric layer is comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

7. The method of claim 1, wherein forming a plurality of openings in said dielectric layer and said BPSG layer comprises performing at least one anisotropic etching process.

8. The method of claim 1, wherein said conductive local interconnect is comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon.

9. A method of forming an SRAM memory cell, comprising:

forming a plurality of transistors above a semiconducting substrate;

depositing a layer comprised of boron phosphosilicate glass (BPSG) above said substrate and said transistors;

depositing a dielectric layer above said BPSG layer, said dielectric layer comprised of a material having a dielectric constant greater than approximately 6.0;

etching a plurality of openings in said dielectric layer and said BPSG layer, each of said openings allowing contact to a doped region of one of said transistors; and

forming a conductive local interconnect in each of said openings.

10. The method of claim 9, wherein depositing said BPSG layer comprises performing at least one of a chemical vapor deposition process and a plasma enhanced chemical vapor deposition process.

11. The method of claim 9, wherein depositing said BPSG layer comprises depositing said BPSG layer to a thickness that ranges from approximately 150-200 nm.

12. The method of claim 9, wherein depositing said BPSG layer comprises depositing said BPSG layer to a thickness such that an upper surface of said BPSG layer extends above a top surface of one of said transistors by approximately 50-100 nm.

13. The method of claim 9, wherein depositing a dielectric layer comprises performing at least one of a chemical vapor deposition process, a plasma enhanced chemical vapor deposition process, an atomic layer deposition process and a spin-coating process.

14. The method of claim 9, wherein said dielectric layer is comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

15. The method of claim 9, wherein etching a plurality of openings in said dielectric layer and said BPSG layer comprises performing at least one anisotropic etching process.

16. The method of claim 9, wherein said conductive local interconnect is comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon.

17. A method of forming an SRAM memory cell, comprising:

forming a plurality of transistors above a semiconducting substrate;

forming a layer comprised of boron phosphosilicate glass (BPSG) above said substrate and between said transistors;

forming a plurality of openings in said BPSG layer, each of said openings allowing contact to a doped region of one of said transistors;

forming a conductive local interconnect in each of said openings;

reducing a thickness of said BPSG layer after said local interconnects are formed; and

forming a dielectric layer above said BPSG layer and between said conductive local interconnects.

18. The method of claim 17, wherein forming said BPSG layer comprises performing at least one of a chemical vapor deposition process and a plasma enhanced chemical vapor deposition process.

19. The method of claim 17, wherein forming said BPSG layer comprises depositing said BPSG layer to a thickness that ranges from approximately 500-1000 nm.

20. The method of claim 17, wherein said dielectric layer is comprised of a material having a dielectric constant greater than approximately 6.0.

21. The method of claim 17, wherein forming said BPSG layer comprises depositing said BPSG layer to a thickness such that an upper surface of said BPSG layer extends above a top surface of one of said transistors by approximately 50-100 nm.

22. The method of claim 17, wherein forming a dielectric layer comprises performing at least one of a chemical vapor deposition process, a plasma enhanced chemical vapor deposition process, an atomic layer deposition process and a spin-coating process.

23. The method of claim 17, wherein said dielectric layer is comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

24. The method of claim 17, wherein forming a plurality of openings comprises performing at least one anisotropic etching process.

25. The method of claim 17, wherein reducing a thickness of said BPSG layer comprises performing at least one etching process to reduce said thickness of said BPSG layer.

26. The method of claim 17, wherein said conductive local interconnect is comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon.

27. A method of forming an integrated circuit device, comprising:

forming a plurality of transistors above a semiconducting substrate;

forming a layer comprised of boron phosphosilicate glass (BPSG) above said substrate and between said transistors;

forming a plurality of openings in said BPSG layer, each of said openings allowing contact to a doped region of one of said transistors;

forming a conductive local interconnect in each of said openings;

reducing a thickness of said BPSG layer after said local interconnects are formed; and

forming a dielectric layer above said BPSG layer and between said conductive local interconnects.

28. The method of claim 27, wherein forming said BPSG layer comprises performing at least one of a chemical vapor deposition process and a plasma enhanced chemical vapor deposition process.

29. The method of claim 27, wherein forming said BPSG layer comprises depositing said BPSG layer to a thickness that ranges from approximately 500-1000 nm.

30. The method of claim 27, wherein said dielectric layer is comprised of a material having a dielectric constant greater than approximately 6.0.

31. The method of claim 27, wherein forming said BPSG layer comprises depositing said BPSG layer to a thickness such that an upper surface of said BPSG layer extends above a top surface of one of said transistors by approximately 50-100 nm.

32. The method of claim 27, wherein forming a dielectric layer comprises performing at least one of a chemical vapor deposition process and a plasma enhanced chemical vapor deposition process.

33. The method of claim 27, wherein said dielectric layer is comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

34. The method of claim 27, wherein forming a plurality of openings comprises performing at least one anisotropic etching process.

35. The method of claim 27, wherein reducing a thickness of said BPSG layer comprises performing at least one etching process to reduce said thickness of said BPSG layer.

36. The method of claim 27, wherein said conductive local interconnect is comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon.

37. The method of claim 27, wherein said integrated circuit device is an SRAM memory cell.

38. A method of forming an SRAM memory cell, comprising:

forming a plurality of transistors above a semiconducting substrate;

depositing a layer comprised of boron phosphosilicate glass (BPSG) above said substrate and between said transistors;

etching a plurality of openings in said BPSG layer, each of said openings allowing contact to a doped region of one of said transistors;

forming a conductive local interconnect in each of said openings;

performing at least one etching process to reduce a thickness of said BPSG layer after said conductive local interconnects are formed; and

forming a dielectric layer above said BPSG layer and between said conductive local interconnects, said dielectric layer being comprised of a material having a dielectric constant greater than approximately 6.0.

39. The method of claim 38, wherein depositing said BPSG layer comprises performing at least one of a chemical vapor deposition process and a plasma enhanced chemical vapor deposition process.

40. The method of claim 38, wherein depositing said BPSG layer comprises depositing said BPSG layer to a thickness that ranges from approximately 500-1000 nm.

41. The method of claim 38, wherein depositing said BPSG layer comprises depositing said BPSG layer to a thickness such that an upper surface of said BPSG layer extends above a top surface of one of said transistors by approximately 50-100 nm.

42. The method of claim 38, wherein forming a dielectric layer comprises performing at least one of a chemical vapor deposition process, a plasma enhanced chemical vapor deposition process, an atomic layer deposition process and a spin-coating process.

43. The method of claim 38, wherein said dielectric layer is comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

44. The method of claim 38, wherein etching a plurality of openings comprises performing at least one anisotropic etching process.

45. The method of claim 38, wherein said conductive local interconnect is comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon.

46. A memory cell, comprising:

a plurality of transistors formed above a semiconducting substrate, each of said transistors comprised of a plurality of doped regions formed in said substrate; and

a plurality of local interconnects, each of which are conductively coupled to a doped region of one of said transistors and positioned in an opening in a layer of boron phosphosilicate glass (BPSG) and a dielectric layer positioned above said BPSG layer, said dielectric layer being comprised of a material having a dielectric constant greater than approximately 6.0.

47. The memory cell of claim 46, wherein said semiconducting substrate is comprised of silicon.

48. The memory cell of claim 46, wherein said doped regions are source/drain regions.

49. The memory cell of claim 46, wherein said BPSG layer has a thickness of approximately 150-200 nm.

50. The memory cell of claim 46, wherein said dielectric layer is comprised of at least one of aluminum oxide, tantalum pentoxide, hafnium oxide and zirconium oxide.

51. The memory cell of claim 46, wherein said local interconnect is comprised of at least one of a metal, a metal alloy, tungsten, copper, aluminum and polysilicon.

52. The memory cell of claim 46, wherein said dielectric layer has a thickness that ranges from approximately 300-850 nm.